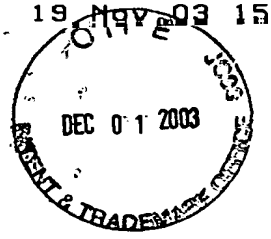

STM226BUS

EXPRESS MAIL NO. EV347012424US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Domenico Pappalardo et al.
Application No.	:	10/050,427
Filed	:	January 15, 2002
For	:	VARIABLE STAGE CHARGE PUMP
Examiner	:	Jennifer M. Dolan
Art Unit	:	2813
Docket No.	:	856063.691
Date	:	November 12, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 35 C.F.R. § 1.131

1. I, Domenico Pappalardo hereby declare as follows. I am a coinventor of U.S. Patent Application No. 10/050,427 entitled "Variable Stage Charge Pump," filed in the United States on January 15, 2002, and claiming priority from U.S. Provisional Application No. 60/277,491 filed on March 20, 2001.

2. I have reviewed U.S. Patent No. 6,504,422 to Rader et al. published on January 7, 2003 and bearing a filing date of November 21, 2000.

3. The invention as presently claimed in claims 1-30 was made prior to November 21, 2000. In particular, the invention had been completed prior to November 21, 2000, as evidenced by the enclosed Exhibits, which will now be explained.

4. Attached hereto as Exhibit A is a patent proposal submitted to the Patent Department at STMicroelectronics S.r.l. in order to proceed with filing a patent application on the completed invention, bearing the title of "Reconfigurable Charge Pump." This original document is in the Italian language because that is the language in which the invention disclosure was submitted for the filing of a patent application. Attached as Exhibit B is a translation into English of the text of the invention disclosure of Exhibit A. Exhibit B is a translation of the text only, and the figures are not included in the translation; instead, at the location of each figure the

translation merely states the figure number and a reference to the Italian language version for the figures is needed.

5. Attached hereto as Exhibit C is a second invention disclosure which bears at the top the title "Charge Pump With Adaptive Stages." Attached as Exhibit D is an English translation of the text of the patent proposal of Exhibit C. The English translation of Exhibit D contains a reference to the figure where the figure is located in the original Italian document and does not contain the figure itself. Accordingly, reference to the figures in Exhibit K is helpful to get a full understanding of the content and text of the patent disclosure together with the English language translation.

6. I have reviewed each of the invention disclosures and state that each of them bears a received date prior to November 21, 2000. In particular, in the upper left-hand corner of the front page of each of the invention disclosures is a line on which the date is printed that the invention disclosures were received by the ST Patent Department. In the original documents of Exhibits A and C, this line is filled in with the date that it was received by the ST Patent Department but it has been blanked out in the copy provided in the Exhibits. This date is prior to November 21, 2000 for each of the invention disclosures. Accordingly, it is clear that we, the inventors had possession of the complete invention as shown and described in the patent application and as currently claimed well prior to November 21, 2000. The invention had been made well prior to invention disclosures being submitted for the patent application and these are submitted as evidence of them being completed.

7. A comparison between the figures of the present application and the figures in the invention disclosure is helpful for an understanding of the completeness of the invention. Figures 1-5 of the invention disclosure of Exhibit C correspond almost exactly to Figures 1-5A of the application as filed. In addition, the tables underneath Figures 3, 4, and 5 of the invention disclosure correspond to Figures 3B, 4B, and 5B of the application as filed. The text describing these figures of the invention disclosure corresponds to the text of the meaning and content of the specification in the application as filed for describing these figures.

8. The Examiner's attention is now directed towards Figures 6-10B of the invention disclosure of Exhibit C. These figures correspond nearly exactly to Figures 7, 8, 9, and 10 of the application as originally filed. This illustrates that the inventors had complete

possession of the invention as described in the specification and shown and had completed the invention prior to November 21, 2000.

9. Exhibit A has Figures 1-6 and accompanying text to describe the circuits, and Figure 7 has the simulation result. Figures 1-6 corresponds to Figures 11-15 as the application was filed. Figure 7 of the invention of the invention disclosure corresponds to Figure 16 of the application as filed, showing the actual simulation results of the circuit in operation. The text, as is clear from the English translation, corresponds to the description of the invention in the application as filed.

10. As can be seen by the close match between the application as filed and the invention disclosures, which had been written well prior to November 21, 2000, and which were actually received by the ST Patent Department prior to November 21, 2000, the invention had been completed prior to November 21, 2000 and the inventors had possession of the claimed invention. The match between the application as filed and the detailed circuit figures, their operation and the equations as found in the invention disclosures of Exhibits A and C is clear and apparent so that a further explanation of the comparison is believed unnecessary.

11. In conclusion, the above two documents, together with their translation, demonstrate a clear understanding of the inventive concept by the inventors well prior to November 21, 2000.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

13-Nov-2003
Date

Domenico Pappalardo
(CO-INVENTOR)

Enclosures:
Exhibits A-D

428791_1.DOC

PATENT PROPOSAL

CHIUSA IN QUANTO ACCORPATA ALLA

*** CONFIDENTIAL ***

Descriptive Title of Invention:

Reconfigurable charge pump

Doc

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EXHIBIT A

Survoltore riconfigurabile

Scopo dell'invenzione.

Oggetto della proposta e' la realizzazione di un survoltore riconfigurabile a due livelli di regolazione, allo scopo di poter utilizzare la stessa struttura per alimentare le principali operazioni ad alta tensione in una memoria EEPROM, con un guadagno d'area pari al 40% rispetto alla soluzione classica che fa uso di due survoltori separati.

Premessa.

Nelle memorie EEPROM e' necessario generare livelli di tensione elevati, rispetto alla tensione di alimentazione, sia per le operazioni di programmazione e di cancellazione (15V), sia per le operazioni di lettura (5V). A tali livelli di tensione, inoltre, e' richiesta anche una determinata capacita di erogazione di corrente (*driving capability*) dell'ordine delle decine di uA per la regolazione a 15V e delle centinaia di uA per la regolazione a 5V.
A tale scopo vengono utilizzati dei survoltori, il cui schema di principio e illustrato nella fig.1.

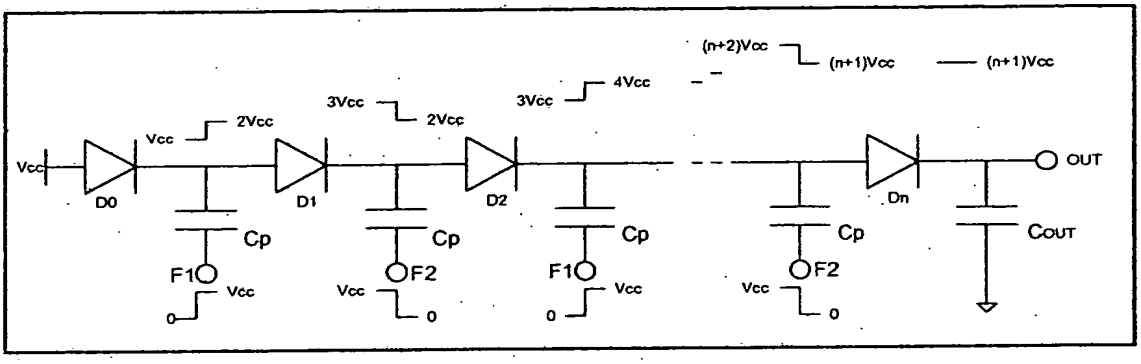

Fig.1 - Schema di principio di un survoltore

Il survoltore della fig.1 soddisfa la equazione eq.1 se si ipotizzano ideali tutti I suoi componenti:

$$I_{out} = C_p f [(n+1)V_{CC} - V_{out}]/n \qquad [eq.1]$$

Dove:
- I_{out} e' la *driving cpability* del survoltore alla tensione V_{out}.
- C_p e' la capacita' survoltrice.
- n e' il numero delle capacita' Cp
- f la frequenza dei segnali, in controfase, F1 e F2

Vi sono molteplici criteri di progetto, ma il piu' seguito e' quello che minimizza l'ingombro, per cui il numero degli stadi e' pari a:

$$n = [2(V_{out} - V_{CC}) / V_{CC}] \qquad [eq.2]$$

Al fine di soddisfare l'eq.1 in un survoltore reale i diodi sono rimpiazzati da una struttura a diodo switch che offre una caduta di qualche decina di mV invece delle centinaia di mV offerti da un semplice diodo. La soluzione circuitale piu' adottata per realizzare un survoltore che soddisfi l'eq.1 e' illustrata in fig.2.

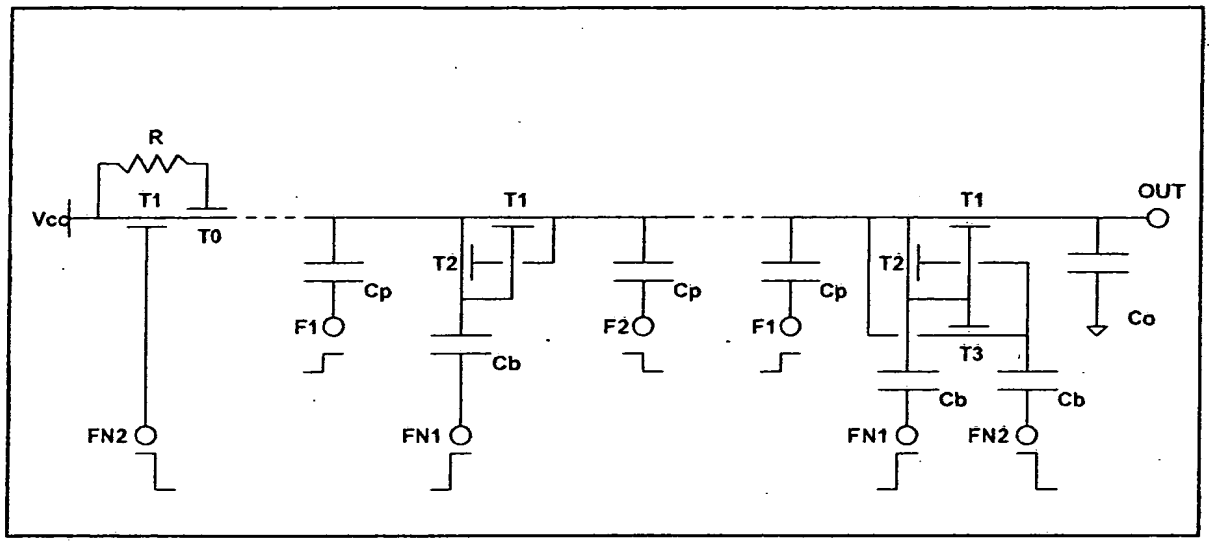

Fig.2 - diodi switch tra stadi di un survoltore

Dove i transistori T1 e T2 sono MOS naturali a bassissima soglia (100mV), in modo che gli ultimi stadi non raggiungano, per effetto body, soglie paragonabili a Vcc.
Il transistore T1 e' opportunamente dimensionato in modo tale che riesca a drenare tutta la corrente da trasferire in meta' periodo del clock e offra una V_{DS} piu' piccola possibile.
Il tansistore T2 serve per riportare T1 in configurazione diodo in inversa quando lo stadio successivo e' survoltato.
La capacita' Cb e' opprortunamente dimensionata in modo da poter trasferire al 90% la differenza di potenziale offerta da FN e quindi dare il giusto "overdrive" al transistore T1 nella fase di trasferimento di carica.
La fase FN e' ad un potenziale doppio rispetto alla fase F, in modo da avere su T1 una $V_{GS}>>V_t$.
Nel collegamento a Vcc tale struttura si semplifica in quanto il primo nodo del sulvoltore varia da Vcc a 2Vcc, quindi basta inserire un diodo T0 e per guadagnare la sua soglia si inserisce il transistore T1 pilotato falla fase FN, in modo tale da far lavorare il diodo solo in inversa.
L'ultimo stadio, invece, e' corredato da una struttura ausiliaria che emula uno stadio successivo in modo da garantire l' "accensione" di T2 durante la fase successiva al trasferimento di carica verso l' uscita.
Dimensionando opportunamente tutti i componenti la struttura di fig.2 soddisfa pienamente l'eq.1 alla frequenza f desiderata.
Due o piu' survoltori possono essere connesi in parallelo per aumentare la driving capability.
In genere si connettono in parallelo due survoltori funzionanti in controfase, in modo tale che alternativamente eroghino corrente in uscita, con il beneficio di raddoppiare la corrente erogata e di ridurre notevolmente la capacita' C_{out} a parita' di *ripple*.
La fig.3 mostra due survoltori in controfase connessi in parallelo.

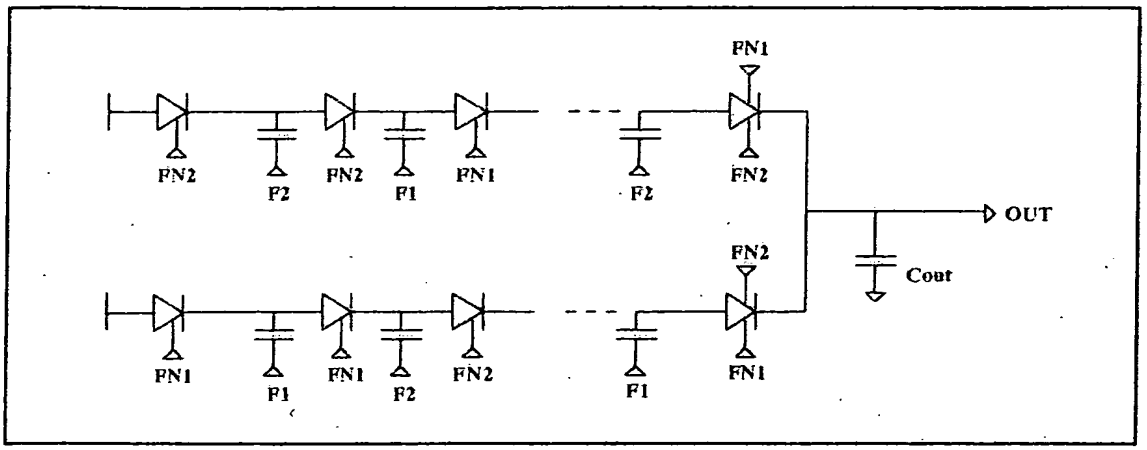

Fig.3 - Survoltori in controfase

Soluzione proposta.

Poiche' l'area occupata da ciascun survoltore non e' indifferente, l'idea e' stata quella di realizzare un solo survoltore che possa essere configurato in modalita' "parallelo" per bassa tensione di regolazione con elevata driving capability e in modalita' "serie" per alta tensione di regolazione con bassa driving capability.
In fig.4 e' mostrato uno schema di principio.

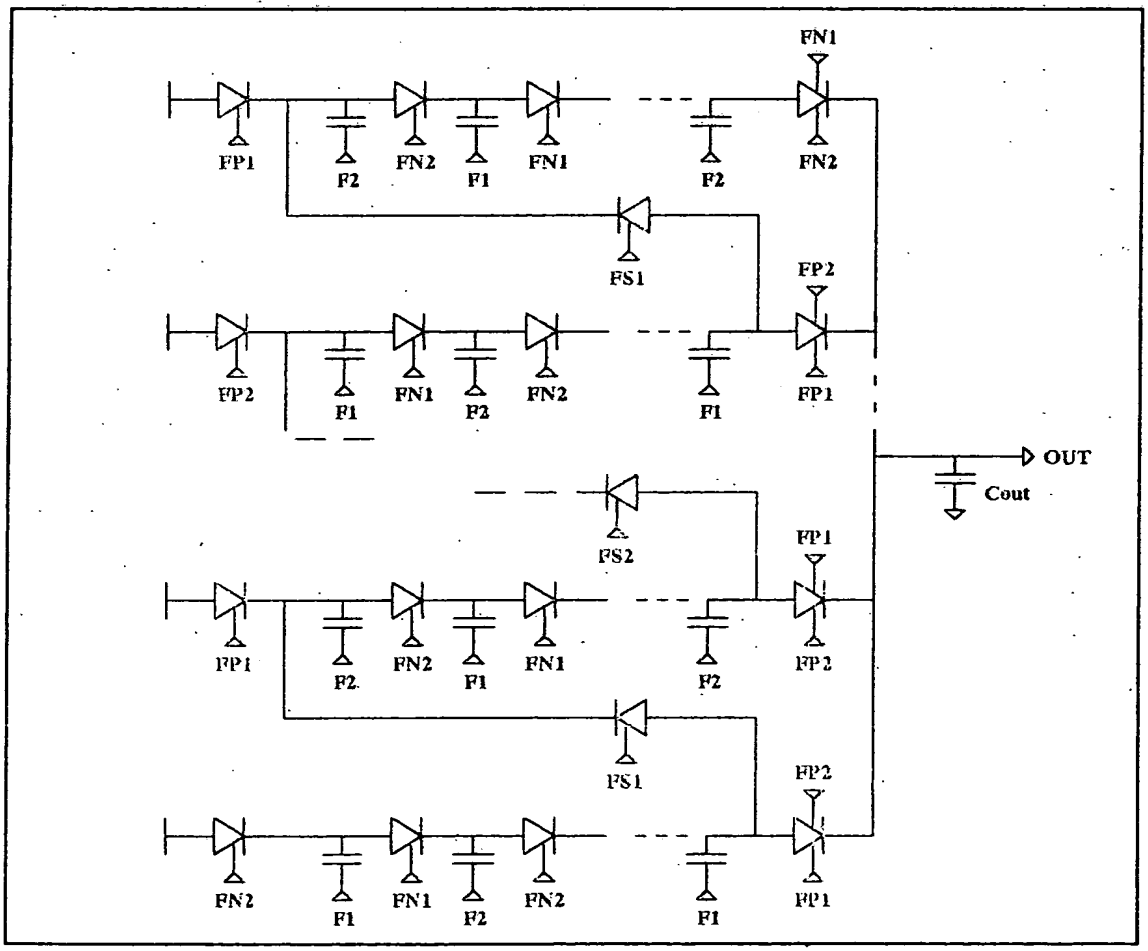

Fig.4 - Survoltore riconfigurabile

Dove FP1 e FP2 coincidono rispettivamente con le fasi survoltate FN1 e FN2, in configurazione "parallelo" , mentre in configurazione "serie" sono a 0V; viceversa per FS1 e FS2.

I diodi switch visualizzati in rosso e in verde nella fig.5 hanno la struttura cicuitale mostrata in fig.5.

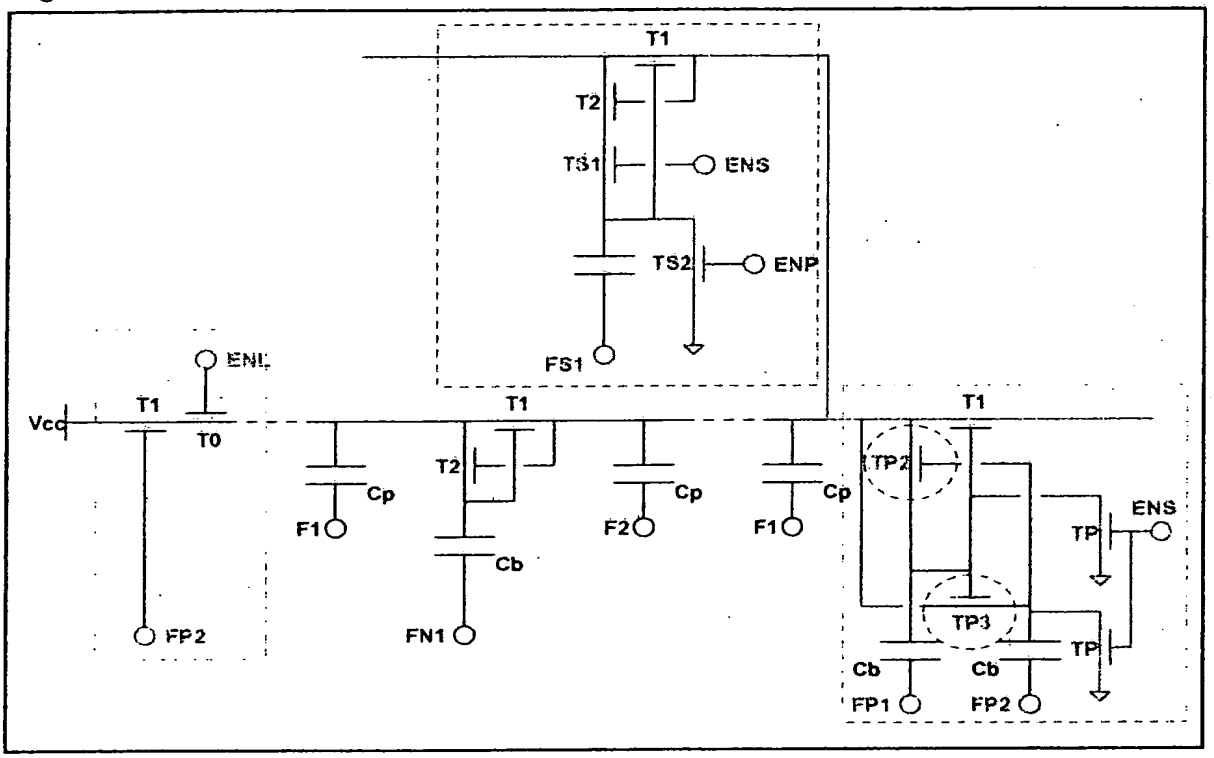

Fig.5 - Diodi switch in configurazione "parallelo" (verde) e in configurazione "serie" (rosso)

Il segnale di controllo ENP e' uguale alla tensione di uscita del survoltore, in configurazione "parallelo", mentre e' uguale a zero in configurazione "serie"; viceversa per il segnale di controllo ENS.
Il segnale ENL e' uguale a Vcc in configurazione "parallelo", mentre e' uguale a zero in configurazione "serie".
Rispetto alla struttura classica dei diodi switch sono stati aggiunti opportuni transistori MOS HV ad alta soglia (600mV) tali da assicurare il completo spegnimento della struttura e non alterarne la funzionalita' quando e' accesa.
Le dimensioni dei transistori TE non sono tali da caricare eccessivamente le capacita' Cb.
I transistori ad alta soglia TP2 e TP3 sostituiscono rispettivamente i transistori a bassa soglia T2 e T3 della struttura classica (vedi fig.3) per evitare percorsi verso *ground* attraverso transistori a bassa soglia.

Funzionalita'.

In configurazione "parallelo" i segnali ENL e ENP son alti, mentre I segnali ENS, FS1 e FS2 sono bassi, in questo modo i transistori T0 e TS2 sono accesi, mentre i transistori TP e TS1 sono spenti.

Lo spegnimento di TS1 garantisce l'interruzione del percorso verso ground, visto che T2 e TS2 sono accesi.
L'accensione di TS2 garantisce lo spegnimento di T1 e quindi l'interruzione del percorso "serie".
La natura dei transistori TS2 e TS3 non comporta nessuna differenza di funzionamento rispetto ad una struttura con transistori a bassa soglia se essi "lavorano" con tensioni abbastanza basse, ma per definizione in configurazione parallelo le tensioni in gioco sono tali che TS2 e TS3 hanno un buon *overdrive*.
In configurazione "serie" il segnale ENS e' alto, mentre i segnali ENL, ENP, FP1 e FP2 sono bassi; in questo modo i transistori TS1 e TP sono accesi, mentre i transistori T0 e TS2 sono spenti.
Il transistore TS1 ha un notevole overdrive visto che e' pilotato dalla tensione di uscita del survoltore e le tensioni ai suoi capi sono, in ogni caso, piu' basse di almeno uno stadio.
Anche le tensioni ai capi di TS2 sono, in ogni caso, ben al di sotto della soglia di breakdown.
I transistori TP accesi assicurano lo spegnimento dei transistori T1, TP2 e TP3 e quindi l'interruzione del percorso "parallelo".

Limiti.

I limiti son dettati essenzialmente dalla tecnologia la quale impone le tensioni di soglia e di breakdown dei transistori. Da questi scaturiscono i limiti sulla tensione di alimentazione Vcc e sul numero degli stadi che si possono attuare.

Realizzazione.

E' stato realizzato un survoltore riconfigurabile in tecnologia F6Y ($1.8V<Vcc<3.6V$ - $Vb_{HV.}=17V$)con leseguenti prestazioni a Vcc=2.3V e f = 10MHz:

Parallelo: $V_{out} = 5.5V$ - $I_{out} = 240uA$
Seriale: $V_{out} = 15V$ - $I_{out} = 60uA$

La soluzione classica, in base alle equazioni eq.1 e eq.2, prevede nei due casi:

1) n = 3 - Cp= 20pF;
2) n = 12 - Cp = 5pF;

La soluzione proposta, in base a quanto detto precedentemente, prevede soltanto n = 12 e Cp = 5pF riconfigurabili secondo lo schema di fig.6

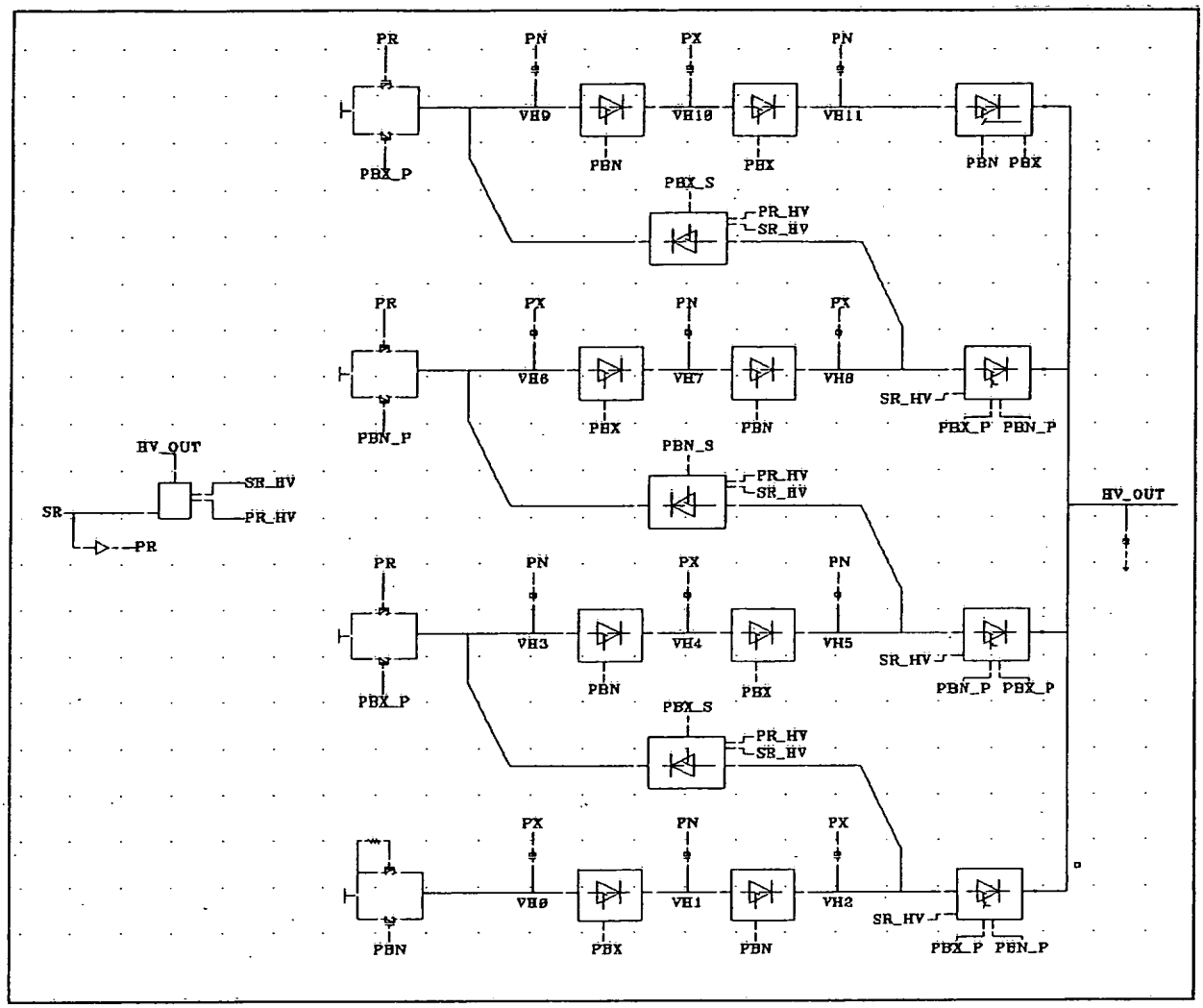

Fig.6 - Survoltore riconfigurabile in tecnologia F6Y

In questo modo in configurazione con SR = 0 si hanno quattro survoltori da tre stadi, a due a due in controfase, connessi in parallelo; mentre con SR = 1 si ha un survoltore da 12 stadi.
I risultati di simulazione, nelle condizioni Vcc=2.3V, f=10MHz e T=27°C, sono mostrati in fig.7.
La funzionalita' di tale circuito e' garantita per tutto il range di alimentazione permessa in tecnologia F6Y, con frequenze minori o uguali a 20MHz e per temperature che vanno da -40°C a 125°C, con una perdita massima , nelle peggiori condizioni, del 10% della sua *driving capability*.

Fig.7 - Simulazione del survoltore riconfigurabile in F6Y

Riconfigurable Booster

Aim of the invention

The present invention also uses a riconfigurable booster having two regulation levels in order to supply the main high voltage operation in an EEPROM memory, with an area gain of 40% with respect to the known solutions using two separated boosters.

Introduction

EEPROM memory devices requires different high voltage levels, with respect to the power supply voltage, to be used during the programming and erasing phases (15V) as well as during the reading phases (5V). Moreover, for these voltage levels a predetermined driving capability is required, for an outputted current of about tens of uA for the 15V regulation, and of about hundreds of uA for the 5V regulation.

In this aim, boosters are provided, whose basic scheme is shown in Figure 1.

Fig. 1

The booster of Figure 1 fits to the following equation (eq.1), only if all components thereof are considered as ideal ones.

$$I_{out} = C_p f [(n+1)V_{CC} - V_{out}]/n \qquad [eq.1]$$

where:

- Iout is the driving capability of the booster for a voltage Vout;
- Cp is the booster capacitor;
- n is the number of the capacitors Cp;
- f is the signal frequency, in opposition of phase F1 and F2.

Different project criteria can be used, but the more applied is the minimization of the circuit size, according to which the number of stages is as follows:

$$n = [2(V_{out} - V_{CC}) / V_{CC}] \qquad [eq.2]$$

In order to fit to eq.1, in a real booster, the diodes are substituted by a switch diode structure, which provides for a voltage fall of some tens of mV, instead of

EXHIBIT B

hundreds of mV as for a simple diode. The more used circuital solution, providing a booster, which fits to eq.1, is shown in Figure 2.

Figure 2

Transistors T1 and T2 are natural MOS transistors having a very low threshold (100mV), in such a way that the final stages do not reach threshold voltages comparable to Vcc, according to the body effect.

Transistor T1 is suitably sized in such a way to let flow all the current to be transferred in a half-clock-period and to provide for a V_{DS} which is as small as possible.

Transistor T2 is used to switch T1 in the diode inverse configuration when the subsequent stage is boosted.

Capacitor Cb is suitably sized in such a way to provide for a transferring of the 90% of the voltage difference provided by FN and thus provide the correct "overdrive" to the transistor T1 during the charge transferring phase.

The FN phase is made at a double voltage value with respect to F phase, in such a way to force on T1 a $V_{GS}>>Vt$.

With respect to the Vcc connection, this structure is simplified, since the booster first node varies from Vcc to 2Vcc, thus requiring only additional diode T0 and, in order to gain a value equal to its threshold voltage, transistor T1 is driven by FN phase, in such a way to force diode operation in the inverted configuration.

On the contrary, the final stage is provided with an auxiliary structure, which emulates a subsequent stage in order to guarantee the switching-on of the transistor T2 during the phase, which follows the charge transferring to the output.

A suitable sizing of all components in the structure of Figure 2 correctly fits to eq.1 for the required frequency f.

Two or more boosters can be connected in parallel in order to increase the driving capability.

Generally speaking, two boosters operating with opposite phases are connected in parallel, in such a way that they alternatively provide an output current, with the

additional advantage of doubling the outputted current and really reducing the capacitor Cout for a same ripple.

Figure 3 shows two boosters operating with opposite phases and connected in parallel.

Figure 3

Proposed solution

Since the area required by each booster is not negligible, the idea is that of providing a single booster which could be configured according to a parallel mode, for low regulation voltage, having a high driving capability, and in a serial mode, for high regulation voltage, having a low driving capability.

Figure 4 shows the basic operation scheme.

Figure 4

FP1 and FP2 correspond to the boosted phases, FN1 and FN2, for the parallel configuration, while they correspond to FS1 and FS2 for 0V.

The switch diodes (shown in red and green in Figure 5) have a circuital structure shown in Figure 5.

Figure 5

The control signal ENP is equal to the output voltage of the booster, according to the parallel configuration, while it is equal to zero according to the serial configuration, the opposite being true for the control signal ENS.

The signal ENL is equal to Vcc according to the parallel configuration, while it is equal to zero according to the serial configuration.

With respect to the known structures for switch diodes, suitable HV MOS transistors have been added, which have a high threshold (600mV) in order to guarantee the complete switching-off of the structure, the operation during the on-phase beings the same.

Transistors TE sizes do not excessively charge the capacitors Cb. Transistors TP2 and TP3, having a high threshold, respectively substitute the low threshold transistors T2 and T3 of the known solution (see Figure 3) in order to avoid paths to ground throughout low threshold transistors.

Operation

When in parallel configuration, signals ENL and ENP are high, while signals ENS, FS1 and FS2 are low. In this way, transistors T0 and TS2 are on, while transistors TP and TS1 are off.

The TS1 switching-off guarantees the path-to-ground cut, since T2 and TS2 are on.

The TS2 switching-on guarantees the T1 switching-off and thus the serial-path cut.

The transistors TS2 and TS3 type does not affect the operating with respect to the structure comprising low threshold transistors, if they work with sufficient low voltages, but, according to their definition, they provide for a good overdrive of TS2 and TS3 for the voltages used according to the parallel configuration.

According to the serial configuration, the signal ENS is high, while signals ENL, ENP, FP1 and FP2 are low. In this way, transistors TS1 and TP are on, while transistors T0 and TS0 are off.

Transistor TS1 shows an high overdrive, since it is driven by the output voltage of the booster and the voltage values at its ends are, in any case, lower for at least one stage.

Also voltage values at the ends of TS2 are, in any case, well lower than the breakdown threshold.

The switching-on of transistors TP guarantees the switching-off of transistors T1, TP2 and TP3 and thus the parallel-path cut.

Limits

The limits are essentially due to the technology, which forces the threshold and breakdown voltages of the transistors. From all this, the limits on the power supply voltage Vcc and on the number of staged that can be realized are due.

Realization

A riconfigurable booster has been realized in technology F6Y (1.8V<Vcc>3.6V - Vb_{HV} = 17V) and the following performances have been obtained for Vcc = 2.3V and f = 10 MHz.

Parallel: V_{out} = 5.5V - I_{out} = 240uA
Serial: V_{out} = 15V - I_{out} = 60uA

The known solution, according to eq.1 and eq.2, has the following results, in the above-listed two cases:

1) n = 3 - Cp= 20pF;
2) n = 12 - Cp = 5pF;

The proposed solution, according to what is above stated, has only n = 12 and Cp = 5pF riconfigurable according to the scheme of Figure 6.

In this way, for the configuration having SR = 0, four boosters with three stages are needed, two by two operating in phase opposition, while for the configuration having SR = 1, only one booster with 12 stages is needed.

The simulation results, for Vcc=2.3V, f=10MHz and T=27°C condition, are shown in Figure 7.

The operating of such a circuit is guarantee in the whole range for the power supply voltage allowed in technology F6Y, with frequencies less or equal than 20MHz and temperature between -40°C and 125°C, showing a maximum loss, in the worst conditions, equal to 10% of its driving capability.

PATENT PROPOSAL

ACORPA LA

*** CONFIDENTIAL ***

Descriptive Title of Invention:

CHARGE PUMP WITH ADAPTATIVE STAGES

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EXHIBIT C

PROPOSTA DI BREVETTO

Charge pump a stadi variabili

1. Introduzione

In certi dispositivi elettronici la tensione d'alimentazione non basta per garantire il buon funzionamento del circuito, in questi casi bisogna disporre di tensioni piu' elevate.

Come ad esempio nel caso delle memorie non volatili programmabili, nel quale, per le operazioni di lettura, programmazione e cancellazione, sono necessarie tensioni fino a 15 volt.

In questi casi, o si fornisce dall'esterno una seconda alimentazione piu' elevata di quella standard, come si faceva sino a qualche anno fa, oppure si generano all'interno dello stesso integrato le tensioni necessarie, come si fa oggi nella maggiorparte dei casi, rendendo cosi' piu' semplice l'uso dell'integrato stesso.

Il circuito in grado di produrre tensioni piu' elevate rispetto a quella d'alimentazione prende il nome di charge pump.

In fig. 1 e' mostrato, in forma semplificata, un charge pump ad N stadi, ognuno dei quali e' costituito da un interruttore e da una capacita' di pumping.

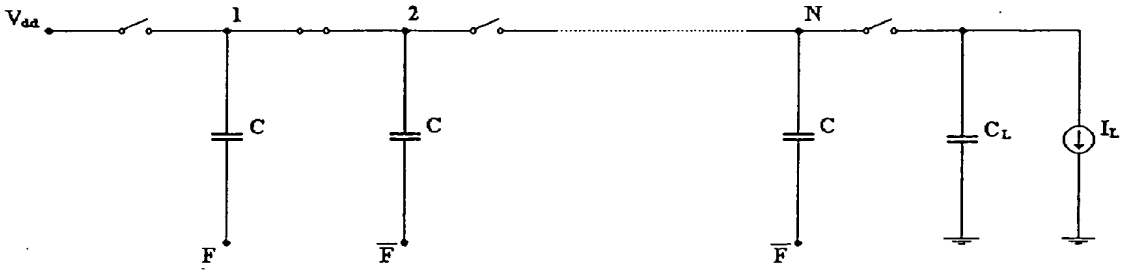


Figura 1

L'area occupata da un charge pump e' piuttosto considerevole ed aumenta al crescere della corrente erogata.

La proposta che viene presentata e' quella di un charge pump a stadi variabili, di un charge pump, cioe', che, fissata l'area occupata, massimizza l'erogazione di corrente scegliendo in modo opportuno il numero dei suoi stadi.

2. Descrizione dell'arte nota

La corrente erogata da un charge pump puo' essere espressa come:

$$I_L = \frac{(N+1)\cdot V_{dd} - V_{OUT}}{N^2} \cdot C_{TOT} \cdot f \qquad (1)$$

Per fare in modo che tale corrente coincida con quella richiesta dal carico si fa variare la frequenza di pumping, f, da 0 Hz fino ad f_{MAX}.
La massima corrente, quindi, che in questo modo si riesce ad ottenere e':

$$I_{LMAX} = \frac{(N+1)\cdot V_{dd} - V_{OUT}}{N^2} \cdot C_{TOT} \cdot f_{MAX} \qquad (2)$$

Essa dipende:

- dal numero di stadi, N, del charge pump, che viene fissato in fase di progetto;
- dalla tensione d'alimentazione, V_{dd}, che puo' assumere un qualunque valore entro un certo range;
- dalla tensione d'uscita, V_{OUT}, il cui valore dipende dal carico che in un certo momento il charge pump sta pilotando;
- dalla capacita' totale C_{TOT}, che e' la somma di tutte le capacita' di pumping, e che occupa la maggiorparte dell'area destinata al charge pump;
- ed infine dalla frequenza f_{MAX}.

Se si vuole massimizzare la corrente che la charge pump puo' erogare, a parita' di occupazione d'area (e quindi di C_{TOT}) e di frequenza massima, f_{MAX}, si potrebbe scegliere opportunamente il numero di stadi N.

Il numero degli stadi in corrispondenza del quale si ha la massima erogazione di corrente (*) e' dato da:

$$N_{OTT} = 2 \cdot \left(\frac{V_{OUT}}{V_{dd}} - 1 \right) \qquad (3)$$

Esso dipende dalla tensione d'alimentazione, V_{dd}, che non e' nota a priori e dalla tensione d'uscita, V_{OUT}, alla quale potrebbe essere richiesto di assumere, in momenti diversi, valori diversi ad esempio per pilotare carichi diversi.

(*) Optimizzation of Word-Line Booster Circuits for Low-Voltage Flash Memories – IEEE Journal of Solid-State Circuits, Vol. 34, No. 8, August 1999.

3. Descrizione del problema e soluzione proposta

Se si vuole che il charge pump sia sempre in grado di erogare la massima corrente possibile, la variabilita' della tensione d'alimentazione, V_{dd}, e della tensione d'uscita, V_{OUT}, rappresenta un problema.

Infatti, come si vede dalla (3), al variare della tensione d'alimentazione, V_{dd}, e della tensione d'uscita, V_{OUT}, varia anche il numero di stadi in corrispondenza del quale la corrente erogata e' massima.

Bisognerebbe allora disporre di un charge pump a stadi variabili, un charge pump, cioe', che sia in grado di riconfigurarsi ogni volta che la tensione d'alimentazione, V_{dd}, o la tensione d'uscita, V_{OUT}, variano, assumendo sempre un numero di stadi che garantisca la massima erogazione di corrente, un numero di stadi, cioe, sempre coerente con la (3).

3.1 Charge pump a stadi variabili

Un charge pump a stadi variabili puo' essere realizzato suddividendo la capacita' totale, C_{TOT}, in un opportuno numero di capacita' di pumping e connettendo queste ultime assieme mediante un'opportuna rete di interruttori fatta in modo che si possa decidere il numero di stadi che il charge pump deve assumere agendo sulle fasi associate alle capacita' di pumping e su quelle che, eventualmente, pilotano gli interruttori.

3.1.1 Esempio di Charge Pump a stadi variabili

A titolo d'esempio in fig. 2 e' mostrata una possibile topologia per un charge pump con numero di stadi variabile tra 1 e 3.

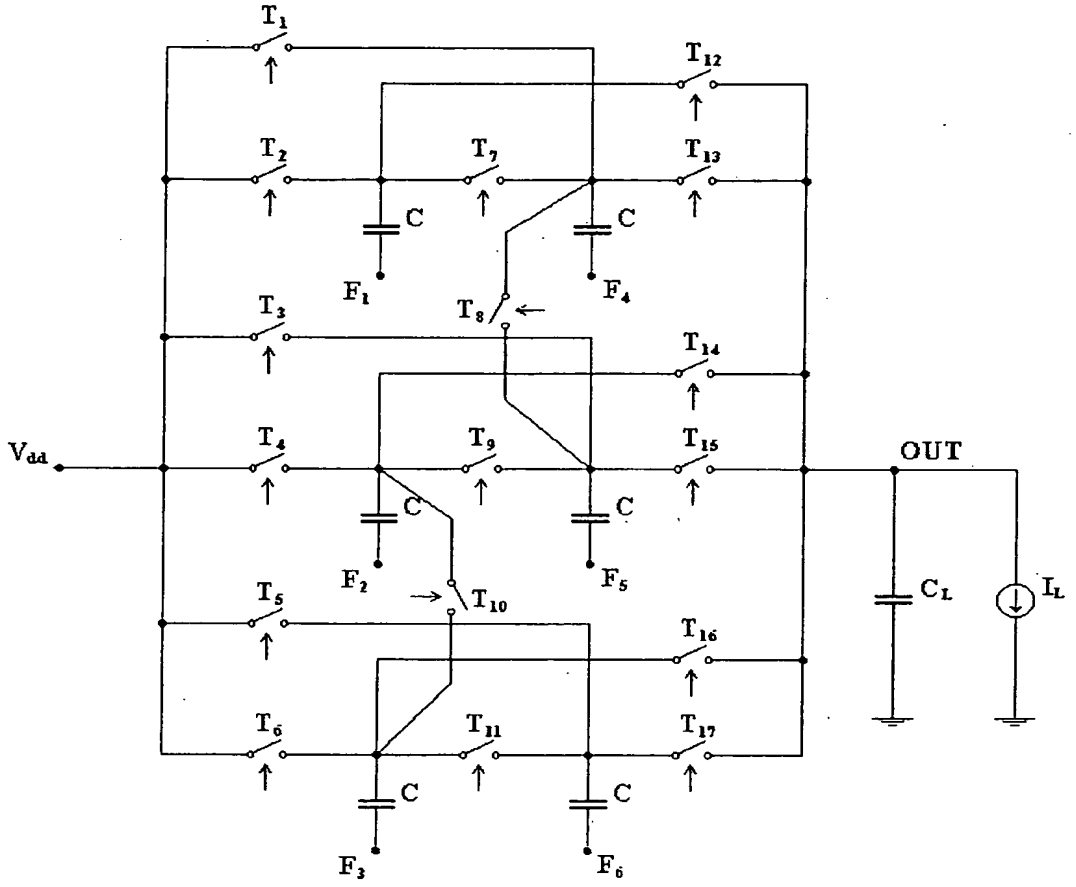


Figura 2

Se si lasciano aperti alcuni interruttori (in grigio in fig. 3) e si pilotano i rimanenti con le fasi riportate in tab. 1, il circuito funziona come un charge pump ad uno stadio costituito da 6 charge pump in parallelo.

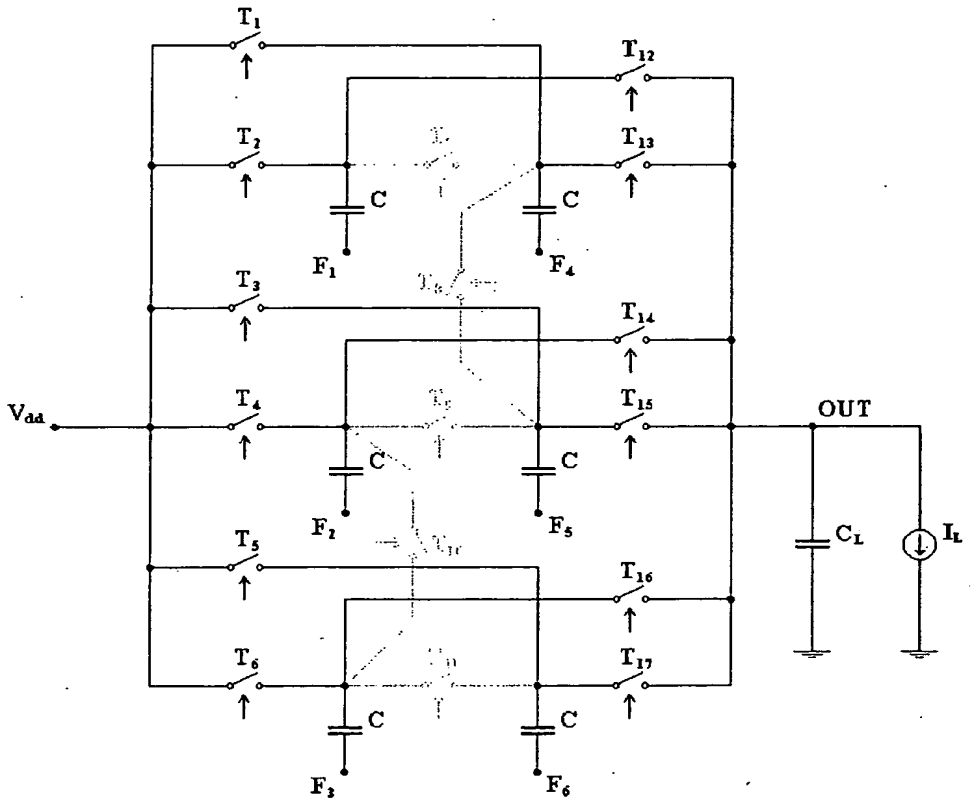


Figura 3

N	F_1	F_2	F_3	F_4	F_5	F_6
1	F	F	F	F	F	F

N	F_{T1}	F_{T2}	F_{T3}	F_{T4}	F_{T5}	F_{T6}	F_{T12}	F_{T13}	F_{T14}	F_{T15}	F_{T16}
1	$\overline{F}$	$\overline{F}$	$\overline{F}$	$\overline{F}$	$\overline{F}$	$\overline{F}$	F	F	F	F	F

Tabella 1

Se invece si pilotano gli interruttori ed i condensatori con le fasi riportate nella tab. 2, il circuito si comporta come un charge pump a due stadi (fig. 4) costituito da 3 charge pump in parallelo.

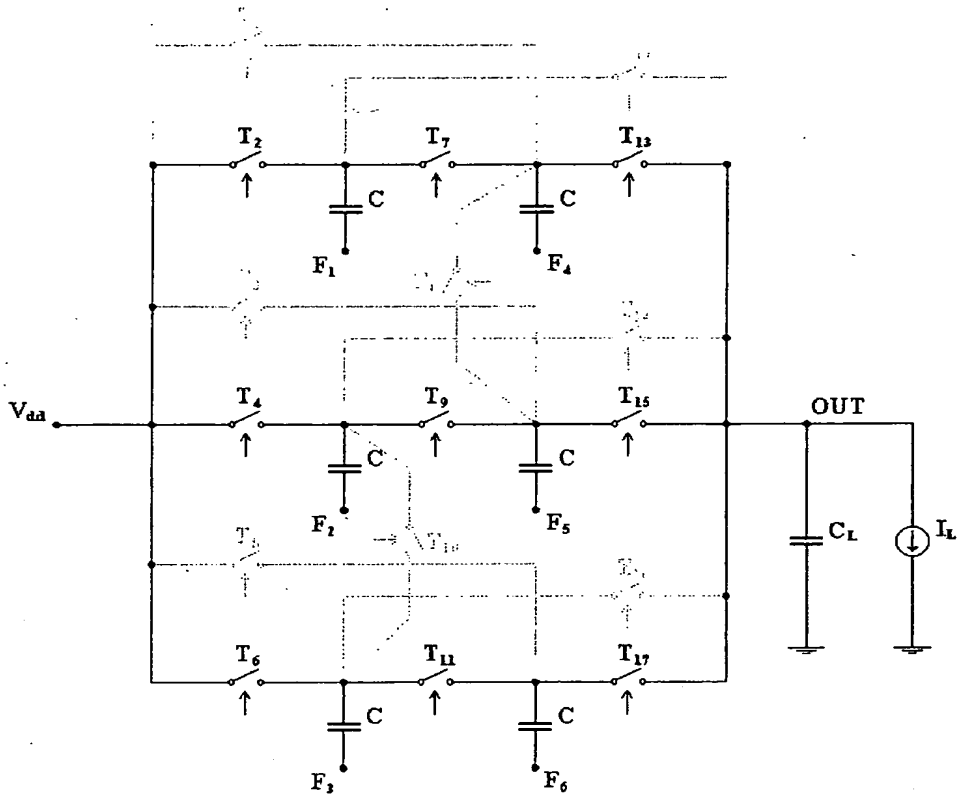


Figura 4

N	F_1	F_2	F_3	F_4	F_5	F_6
2	F	F	F	$\overline{F}$	$\overline{F}$	$\overline{F}$

N	F_{T2}	F_{T4}	F_{T6}	F_{T7}	F_{T9}	F_{T11}	F_{T13}	F_{T15}	F_{T17}
2	$\overline{F}$	$\overline{F}$	$\overline{F}$	F	F	F	$\overline{F}$	$\overline{F}$	$\overline{F}$

Tabella 2

Infine se si pilotano gli interruttori ed i condensatori con le fasi riportate nella tab. 3, il circuito diviene un charge pump a tre stadi (fig. 5) costituito da 2 charge pump in parallelo.

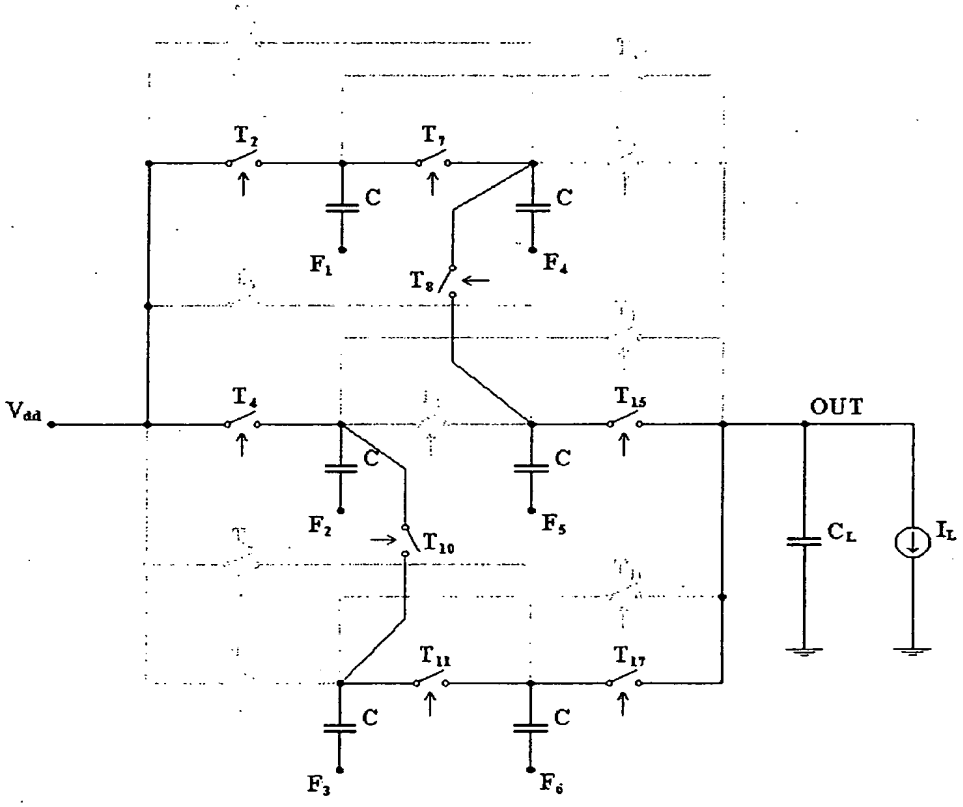


Figura 5

N	F_1	F_2	F_3	F_4	F_5	F_6
3	F	F	$\overline{F}$	$\overline{F}$	F	F

N	F_{T2}	F_{T4}	F_{T7}	F_{T8}	F_{T10}	F_{T11}	F_{T15}	F_{T17}
3	$\overline{F}$	$\overline{F}$	F	$\overline{F}$	F	$\overline{F}$	F	F

Tabella 3

3.2 Circuiti di controllo

Un charge pump a stadi fissi o variabili non e' in grado di funzionare da solo, ma ha bisogno di diversi altri sottocircuiti: i circuiti di controllo.

In fig. 6 e' mostrato un esempio di diagramma a blocchi di un charge pump completo, in grado, cioe', di funzionare autonomamente.

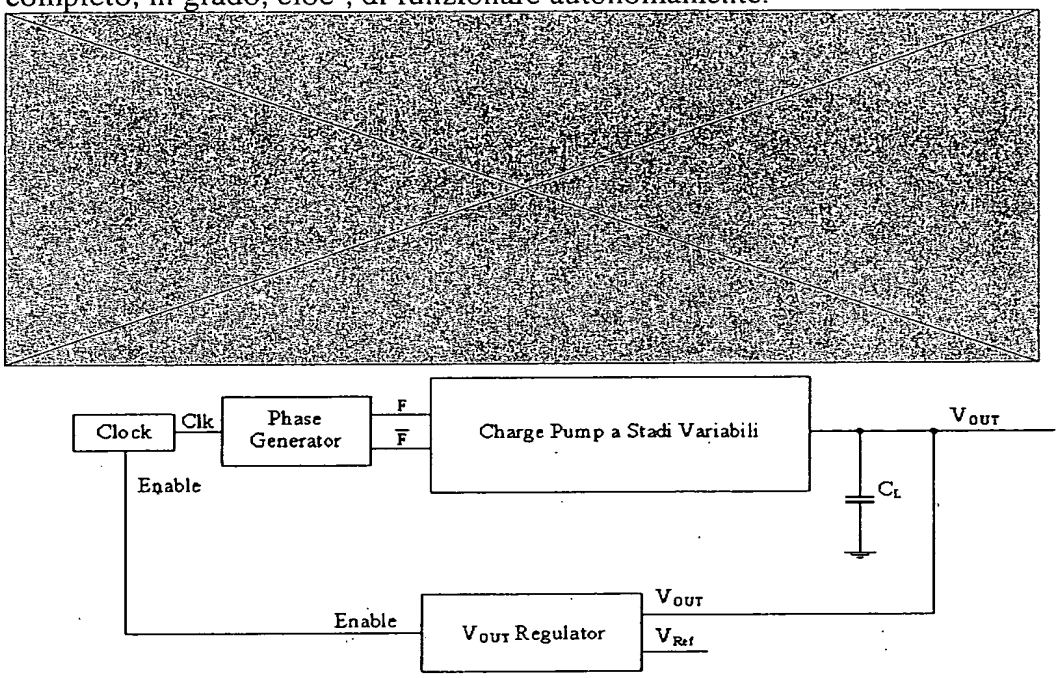


Figura 6

In esso sono presenti:

- Il Clock Generator.
- Il Phase Generator, che produce le fasi necessarie per pilotare interruttori e condensatori di pumping.
- Ed infine il V_{OUT} Regulator, il quale si preoccupa di mantenere la tensione d'uscita il piu' possibile prossima ad un valore fissato.

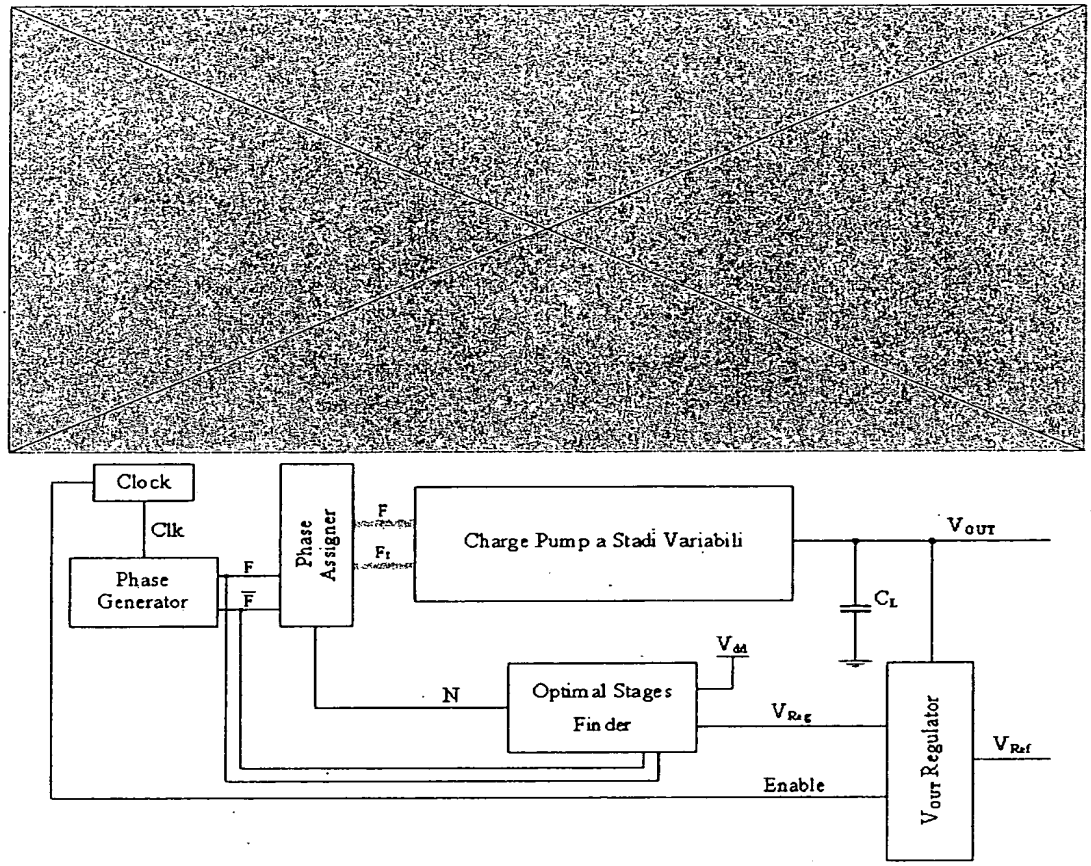


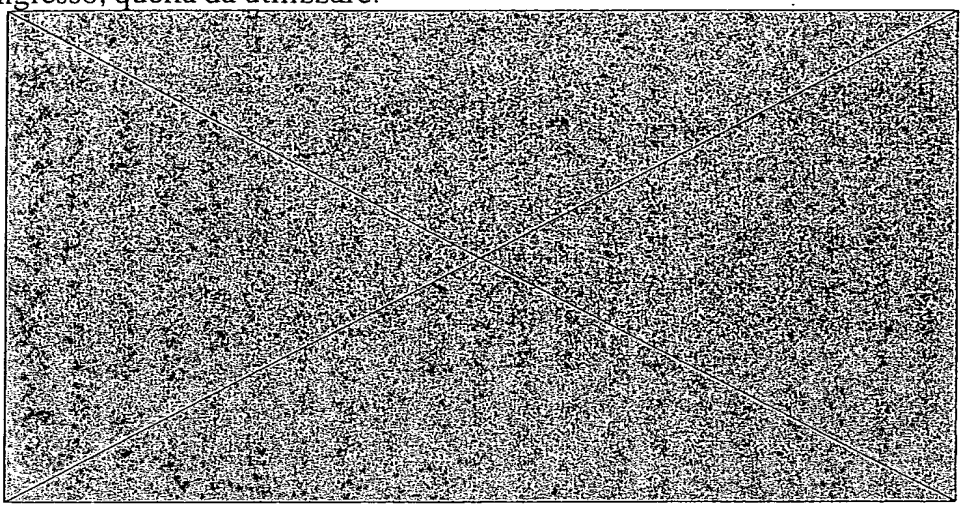
Figura 7

In un charge pump a stadi variabili sono necessari altri due sottocircuiti , come si puo' vedere nel diagramma a blocchi mostrato, a titolo d'esempio, in fig. 7:

- Il Phase Assigner, che assegna le fasi prodotte dal Phase Generator, agli interruttori ed ai condensatori di pumping in modo da realizzare un charge pump avente il numero stadi desiderato.
- L'Optimal Stages Finder, il quale facendo uso della tensione d'alimentazione, V_{dd}, e della tensione d'uscita, V_{OUT}, (o della tensione di regolazione, V_{REG}), ricevute in ingresso, restituisce in uscita il numero di stadi che garantisce la massima erogazione di corrente.

3.2.1 Esempio di Phase Assigner

Il Phase Assigner potrebbe essere costituito, ad esempio, da tanti multiplexer quante sono le fasi che pilotano i condensatori di pumping e gli interruttori (fig. 8), utilizzando per ognuno il numero degli stadi per selezionare, tra le fasi in ingresso, quella da utilizzare.



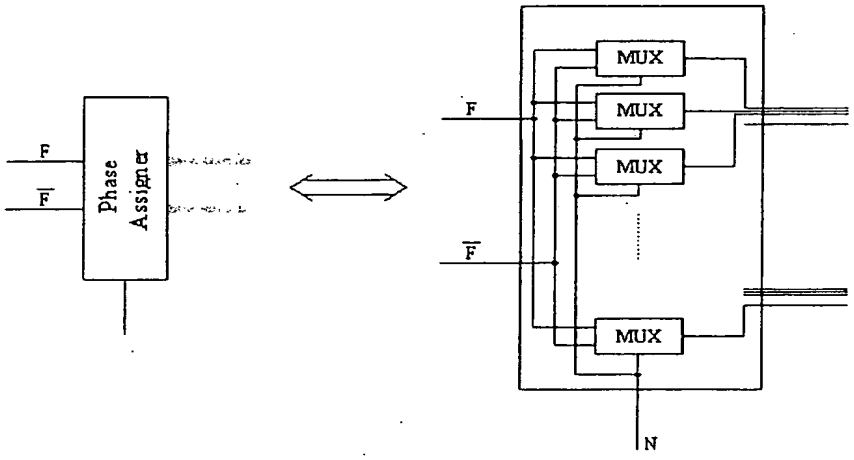


Figura 8

3.2.2 Esempio di Optimal Stages Finder

Facendo uso della (3) e' possibile determinare il numero degli stadi ottimo al variare del rapporto $\frac{V_{OUT}}{V_{dd}}$, come si puo' vedere, ad esempio, in fig. 9 nel caso in cui V_{dd} varia tra 1.5 e 3.7 V, e $V_{OUT} = 5V$.

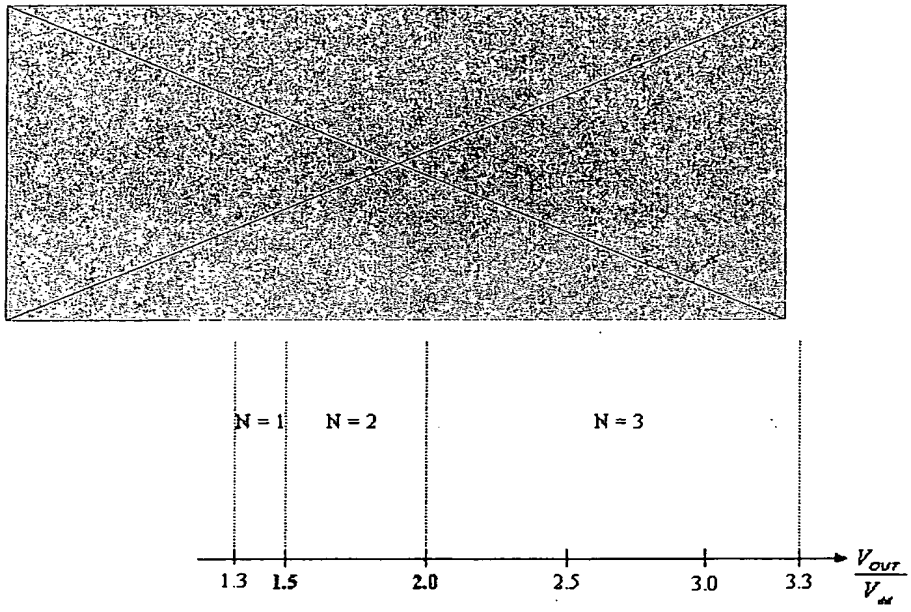


Figura 9

Dalla fig. 9 risulta chiaro che e' sufficiente sapere come e' il rapporto $\frac{V_{OUT}}{V_{dd}}$ rispetto a 1.5 e 2.0 per risalire al valore ottimo di N.

Una possibile realizzazione dell'Optimal Stages Finder puo' quindi comprendere (fig. 10) alcuni comparatori (due in questo caso) ed un circuito logico in grado di convertire i valori in uscita dai comparatori nel valore binario di N_{OTT} (tab. 4).

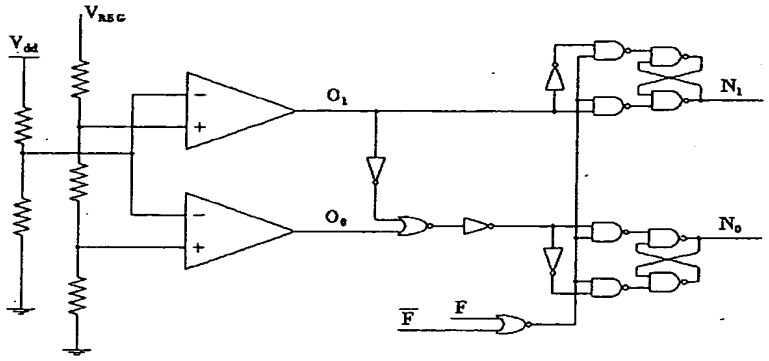


Figura 10

$\left(\frac{V_{OUT}}{V_{dd}}\right)_{MIN}$	$\left(\frac{V_{OUT}}{V_{dd}}\right)_{MAX}$	O_1	O_0	N_1	N_0
1.3	1.5	0	0	0	1
1.5	2.0	1	0	1	0
2.0	3.3	1	1	1	1

Tabella 4

PATENT PROPOSAL

Variable stages charge pump

1. Introduction

In some electronic devices, the voltage power supply does not guarantee the correct operation of the circuit. In such a case, higher voltages are required.

This is the case, for example, of programmable non-volatile memory devices, where the reading, programming and erasing operations needs voltage values up to 15 V.

In these cases, a second power supply, higher than the standard one, can be furnished from outside the circuit - the only solution till a few years ago, or the required voltages are generated inside the integrated circuit - now the more used solution, thus obtaining a simpler use of the IC.

The circuit that can provide higher voltages than the power supply one is usually called charge pump.

Figure 1 shows, in a simplified manner, an N stages charge pump, each stage comprising a switching and a pumping capacitors.

Figure 1

The integration area of the charge pump is really large and it increases when the outputted current grows.

The proposal hereinbelow described relates to a variable stages charge pump, i.e. a charge pump that maximizes, the integration area having been fixed, the output of current, by choosing, in an opportune way, the number of its stages.

2. Prior Art description

The current outputted from a charge pump could be determined as follows:

$$I_L = \frac{(N+1)\cdot V_{dd} - V_{OUT}}{N^2} \cdot C_{TOT} \cdot f \qquad (1)$$

In order to make such a current equal to the current required by the load, the pumping frequency, f, is varied from 0 Hz to f_{MAX}.

Exhibit D

So, the maximum current value thus obtained is:

$$I_{LMAX} = \frac{(N+1)\cdot V_{dd} - V_{OUT}}{N^2} \cdot C_{TOT} \cdot f_{MAX} \qquad (2)$$

It depends on:

- the number N of the charge pump stages, which is to be fixed during the project phase
- the power supply voltage, Vdd, which can be of any value within a given range;
- the output voltage, Vout, whose value is related to the load driven in a given time by the charge pump;
- the total capacitive value C_{TOT}, which is the sum of all pumping capacitors and requires the large part of the integration area of the charge pump; and
- the frequency f_{MAX}.

In order to maximize the outputted current from the charge pump, with the same amount of occupied area (and thus the same C_{TOT}) and with the same maximum frequency, f_{MAX}, the stages number N can be opportunely chosen.

The stages number for which the outputted current has the maximum value (*) is as follows:

$$N_{OTT} = 2 \cdot \left(\frac{V_{OUT}}{V_{dd}} - 1 \right) \qquad (3)$$

It depends on the power supply voltage, Vdd, which is not known *a priori* and the output voltage, V_{OUT}; which can have, in different time, different values, in order to drive, for example, different loads.

(*) Optimization of Word-Line Booster Circuits for Low-Voltage Flash Memories – IEEE Journal of Solid-State Circuits, Vol. 34, No. 8, August 1999.

3. Problem description and proposed solution

In order to provide a charge pump able to output the maximum possible current amount, the main problems are due to the variability of the power supply voltage, Vdd, and the output voltage, V_{OUT}.

In fact, starting from the above-listed formula (3), it can be seen that when the power supply voltage, Vdd, and the output voltage, V_{OUT}, vary, also the stages number, in relation with the maximum amount of the outputted current, varies.

A variable stages charge pump will be useful, which is able to reconfigure any time the power supply voltage, Vdd, or the output voltage, V_{OUT}, vary, the stages number always providing the maximum outputted current amount, in other word, a stages number always coherent with formula (3).

3.1 Variable stages charge pump

A variable stages charge pump can be obtained by dividing a total capacitor, C_{TOT}, into a suitable number of pumping capacitors and connecting such pumping capacitors together through a suitable switching network, which is made in such a way to decide the number of stages for the charge pump by acting on the pumping capacitors frequencies and on the switching drivers capacitors frequencies.

3.1.1 Variable stages charge pump example

By way of a non-limitative example, a possible charge pump layout is shown in Figure 2, such a layout having a number of stages between 1 and 3.

Figure 2

If the switches shown in gray in Figure 3 are kept open and the remaining switches are driven by means of the phases values according to Table 1, the shown circuit does work as a charge pump having a single stage with 6 charge pumps in parallel.

Figure 3

N	F_1	F_2	F_3	F_4	F_5	F_6
1	F	F	F	F	F	F

N	F_{T1}	F_{T2}	F_{T3}	F_{T4}	F_{T5}	F_{T6}	F_{T12}	F_{T13}	F_{T14}	F_{T15}	F_{T16}
1	$\overline{F}$	$\overline{F}$	$\overline{F}$	$\overline{F}$	$\overline{F}$	$\overline{F}$	F	F	F	F	F

Table 1

On the contrary, if the switches and the capacitors are driven by means of the phases value according to Table 2, the shown circuit does work as a charge pump having two stages (as shown in Figure 4) with 3 charge pumps in parallel.

Figure 4

N	F_1	F_2	F_3	F_4	F_5	F_6
2	F	F	F	$\overline{F}$	$\overline{F}$	$\overline{F}$

N	F_{T2}	F_{T4}	F_{T6}	F_{T7}	F_{T9}	F_{T11}	F_{T13}	F_{T15}	F_{T17}
2	$\overline{F}$	$\overline{F}$	$\overline{F}$	F	F	F	$\overline{F}$	$\overline{F}$	$\overline{F}$

Table 2

Finally, if the switches and the capacitors are driven by means of the phases values according to Table 3, the shown circuit does work as a charge pump having three stages (as shown in Figure 5) with 2 charge pumps in parallel.

Figure 5

N	F_1	F_2	F_3	F_4	F_5	F_6
3	F	F	$\overline{F}$	$\overline{F}$	F	F

N	F_{T2}	F_{T4}	F_{T7}	F_{T8}	F_{T10}	F_{T11}	F_{T15}	F_{T17}
3	$\overline{F}$	$\overline{F}$	F	$\overline{F}$	F	$\overline{F}$	F	F

Table 3

3.2 Control circuits

A charge pump with fixed or variable stages cannot work alone, but requires different other circuits: the control circuits, indeed.

Figure 6 shows as an example a block diagram of a complete charge pump, i.e. a complete circuit able to work with autonomy.

Figure 6

The circuit comprises:
- the Clock Generator;
- the Phase Generator, which provides for the required phases to drive the switches and the pumping capacitors; and
- the V_{OUT} Regulator, which maintains the output voltage at a fixed value in the best possible way.

Figure 7

A charge pump with variable stages needs two additional circuits, as shown in the block diagram of Figure 7, given by way of an example.

- The Phase Assigner, which assigns the phases given by the Phase Generator to the switches and pumping capacitors in such a way to provide for a charge pump having the desired number of stages;
- The Optimal Stages Finder, which uses the power supply voltage, Vdd, and the output voltage, V_{OUT} (or a regulation voltage, V_{REG}), received at its inputs, and provides the number of stages which guarantees the maximum output current.

3.2.1 Phase Assigner Example

The Phase Assigner can be made, for example, by means of a number of multiplexers equal to the pumping capacitors and switches driving phases (Figure 8), for each multiplexer the number of stages being used for selecting, within the input phases, the phase to be used.

Figure 8

3.2.2 Optimal Stages Finder Example

Using the formula (3), it is possible to define the optimal number of stages when the $\frac{V_{OUT}}{V_{dd}}$ rate varies, as shown, by way of an example, in Figure 9, in the instance of V_{dd} varying between 1.5 and 3.7 V, and $V_{OUT} = 5V$.

Figure 9

From Figure 9, it is clear that knowing of the $\frac{V_{OUT}}{V_{dd}}$ ratio with respect to 1.5 and 2.0 does suffice to obtain the optimal value of N.

A possible embodiment of the Optimal Stages Finder does comprise (Figure 10) some comparators (in the instance, two) and a logic circuit which is able to convert the comparators output values in the binary value N_{OTT} (Table 4).

Figure 10

$\left(\frac{V_{OUT}}{V_{dd}}\right)_{MIN}$	$\left(\frac{V_{OUT}}{V_{dd}}\right)_{MAX}$	O_1	O_0	N_1	N_0
1.3	1.5	0	0	0	1
1.5	2.0	1	0	1	0
2.0	3.3	1	1	1	1

Table 4